REMARKS

These remarks are set forth in response to the Final Office Action mailed September 20, 2004 (the "Office Action"). As this amendment has been timely filed within the three-month statutory period, neither an extension of time nor a fee is required. Presently, claims 1-20 are pending in the Patent Application. Claims 1-20 have been rejected under 35 U.S.C. §103(a). The objections and rejections are set out in more detail below.

I. Brief Review of Applicants' Invention

Prior to addressing the rejections on the art, a brief description of the present invention is appropriate. The present invention relates to a method and apparatus for high speed interprocess communications ("IPC"). In conventional IPC, multiple processes can communicate with one another via the use of a shared region of random access memory ("RAM") to which each process can write data, and from which each process can read data. When communicating through the shared region of RAM, a first process functioning as a message source can write a message to the shared region of RAM. Subsequently, a second process, functioning as a message receiver, can read the written message from the shared region of RAM. Thus, at a minimum, two system calls are required to move n bytes of data from the first process to the second process through the shared region of RAM. Moreover, 2*n bytes of data will be stored in total: n bytes into the shared region of RAM, and n bytes into user memory space associated with the second process.

To overcome the excessive overhead associated with conventional IPC utilizing a shared region of RAM, the high speed IPC method and apparatus of the present invention avoids moving 2*n bytes of data by passing from the first process directly to a message list of the second process a memory offset which is used by the second process to access the data. The second process then can manipulate and modify the data in place within the shared region of RAM. Accordingly, it is not required that the data be copied from the shared region of RAM to an alternate location while the manipulation takes place, thereby improving system efficiency.

II. Claim Rejections on the Art

Presently, claims 1 through 20 are pending in the subject patent application (the "Application"). In the Office Action, however, each of claims 7 and 9 -12 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,181,707 to Erickson et al. ("Erickson") in view of U.S. Patent No. 5,504,901 Peterson ("Peterson"). Claims 1-6, 8 and 13-18 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Erickson in view of Peterson, and in further view of U.S. Patent No. 6,148,377 to Carter et al. ("Carter"). Finally, claims 19 and 20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Erickson in view of Peterson, in view of Carter, and in further view of U.S. Patent No. 5,991,845 to Bohannon et al. ("Bohannon").

Referring to amended claims 1, 7 and 13, each of the claims recites the limitation of the first process adding to a message list corresponding to the second process a memory offset which corresponds to the location of data in the message buffer. None of the cited references teach or suggest this limitation. Erickson, in particular, loads an offset into its CDCC's Word-In-Queue Register. The CDCC's transmit hardware portion offsets the base address of its transmit queue with the Word-In-Queue Register and uses that combined address to fetch the first word of the message from its own transmit queue in dual-port RAM. The Word-In-Queue is then regenerated at the receiver. (Col. 7, lines 44-55). Such a process requires many more steps and is far more resource intensive than the claimed method of high speed interprocess communication.

Peterson also does not teach or suggest a first process adding a memory offset to a message list of a second process. Instead, Peterson incorporates a value of an offset pointer into instructions of a call sequence. The value of the memory offset pointer is used when the call sequence is executed. Col. 9, lines 7-13. Accordingly, the call sequence must be executed before the data in the shared memory can be accessed. In contrast, the second process of the claimed invention can access the shared data at any time since the memory offset is contained in its message list. Consequently, claims 1, 7 and 13 are distinguishable from the cited art. Claims 2-6, 8-

12 and 14-20 are believed to be allowable at least by virtue of their dependence on allowable base claims.

III. Conclusion

Applicant has made every effort to present claims which distinguish over the prior art, and it is believed that all claims are in condition for allowance. Nevertheless, Applicant invites the Examiner to call the undersigned if it is believed that a telephonic interview would expedite the prosecution of the application to an allowance. In view of the foregoing remarks, Applicant respectfully requests reconsideration and prompt allowance of the pending claims.

Respectfully submitted,

Date: 11-30-04

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